Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (previously presented): A system comprising:

a digital signal processor comprising a bus connectable to a memory; and

a butterfly coprocessor coupled to the digital signal processor to perform an operation scheduled by the digital signal processor.

Claim 2 (previously presented): The system of claim 1, wherein the digital signal processor further comprises:

a data address generator coupled to the bus to address the memory on behalf of a requesting device.

Claim 3 (previously presented): The system of claim 2, wherein the digital signal processor further comprises an arithmetic unit to perform arithmetic operations in the digital signal processor.

Claim 4 (previously presented): The system of claim 3, wherein the arithmetic unit further comprises a branch metric unit to perform branch metric calculations.

Claim 5 (previously presented): The system of claim 4, wherein the arithmetic unit further comprises one or more registers to which the branch metric unit may store one or more results.

Claim 6 (previously presented): The system of claim 5, further comprising one or more registers in the arithmetic unit addressable by the data address generator.

Claim 7 (previously presented): The system of claim 1, wherein the butterfly coprocessor further includes a plurality of butterfly units to perform butterfly operations.

Claim 8 (previously presented): The system of claim 7, wherein the butterfly operations are parallel operations.

Claim 9 (previously presented): The system of claim 8, wherein the plurality of butterfly units in the butterfly coprocessor are coupled to further perform add-compare-select operations at the direction of the digital signal processor.

Claim 10 (previously presented): The system of claim 8, wherein the plurality of butterfly units in the butterfly coprocessor are coupled to further perform approximations of logarithmic sum exponential operations at the direction of the digital signal processor.

Claim 11 (previously presented): The system of claim 8, wherein the data address generator is coupled to access a path metric retrieved from a path metric memory.

Claim 12 (previously presented): The system of claim 11, wherein the data address generator of the digital signal processor is coupled to retrieve a branch metric from the branch metric unit.

Claims 13-20 (canceled)

Claim 21 (currently amended): A system comprising:

a digital signal processor~~, comprising~~ including:

a bus connectable to a memory;

a data address generator; and

an arithmetic unit; and

a butterfly coprocessor coupled to the digital signal processor to perform an operation scheduled by the digital signal processor.

Claim 22 (previously presented): The system of claim 21, wherein the digital signal processor further comprises a software program which, upon execution, causes the system to:

identify a stage of a trellis diagram;

identify a number of nodes in the stage; and

identify a number of branches extending from each node.

Claim 23 (original): The system of claim 22, wherein the butterfly coprocessor further comprises a plurality of butterfly units.

Claim 24 (original): The system of claim 23, wherein the number of butterfly units equals the number of nodes in the stage.

Claim 25 (previously presented): The system of claim 24, wherein the butterfly coprocessor is coupled to compute path metrics for the stage.

Claim 26 (previously presented): The system of claim 25, wherein the butterfly units are coupled to simultaneously compute a path metric for each node of the stage.